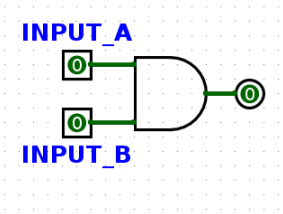
CS 61C Spring 2019

SDS, FSMs

Discussion 5: February 27, 2019

1 State Intro

There are two basic types of circuits: combinational logic circuits and state elements. **Combinational logic** circuits simply change based on their inputs after whatever propagation delay is associated with them. For example, if an AND gate (pictured below) has an associated propagation delay of 2ps, its output will change based on its input as follows:



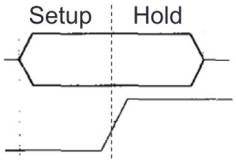
input a	2L 4H 3L 2H 2L 1H 5L 1H 1L 1H 2L
input b	2L 4H 3L 2H 2L 1H 5L 1H 1L 1H 2L
output	2U 2L 4H 3L 2H 2L 1H 5L 1H 1L 1H

Where U, L, and H refer to an undefined, low (0), or high (1) signal respectively, for some number of nanoseconds.

You should notice that the output of this AND gate always changes 2ps after its inputs change.

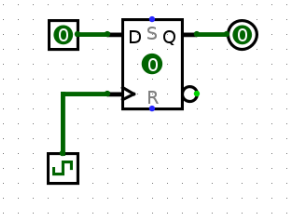
State elements, on the other hand, can *remember* their inputs even after the inputs change. State elements change value based on a clock signal. A rising edge-triggered register, for example, samples its input at the rising edge of the clock (when the clock signal goes from 0 to 1).

Like logic gates, registers also have a delay associated with them before their output will reflect the input that was sampled. This is called the **clk-to-q** delay. ("Q" often indicates output). This is the time between the rising edge of the clock signal and the time the register's output reflects the input change.



The input the register samples has to be stable for a certain amount of time around the rising edge of the clock for the input to be sampled accurately. The amount of time before the rising edge the input must be stable is called the **setup** time, and the time after the rising edge the input must be stable is called the **hold** time. Hold time is included in clk-to-q delay, so clk-to-q time will always be greater than or equal to hold time.

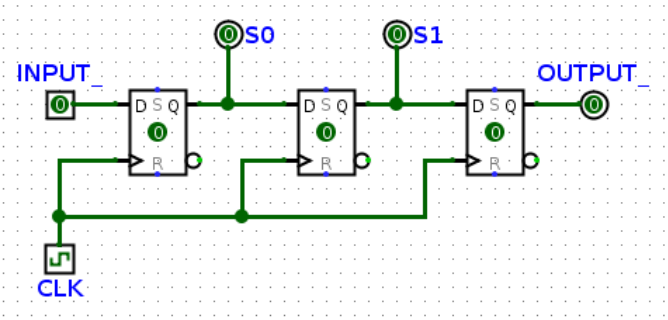
For the following register circuit, assume **setup** of 2.5ps, **hold** time of 1.5ps, and a **clk-to-q** time of 1.5ps. The clock signal has a period of 13ps.



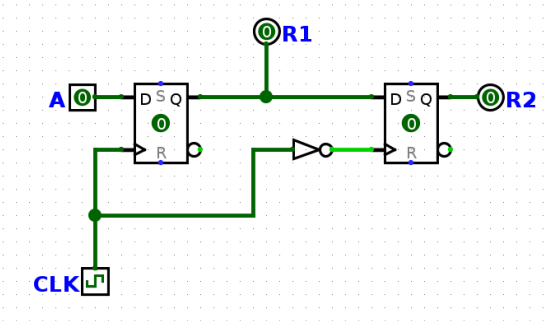
clock 6.5L 6.5H 6.5L 6.5H
input 1L 2H 1L 5H 3L 2H 2L 1H 5L 1H 3L
output 8U 13H 5L

You'll notice that the value of the output in the diagram above doesn't change immediately after the rising edge of the clock. Clock cycle time must be small enough that inputs to registers don't change within the hold time and large enough to account for clk-to-q times, setup times, and combinational logic delays.

1.1 For the following 2 circuits, fill out the timing diagram. The clock period (rising edge to rising edge) is 8ps. For every register, clk-to-q delay is 2ps, setup time is 4ps, and hold time is 2ps. NOT gates have a 2ps propagation delay

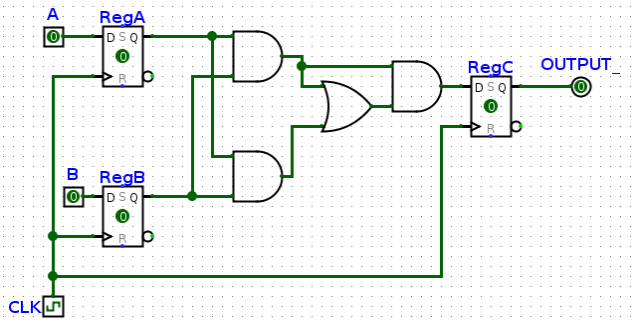


clk 4L 4H 4L 4H 4L 4H 4L 4H 4L 4H 4L 4H
in 14L 4H 6L 16H 8L
s0
s1
out



clk 4L 4H 4L 4H 4L 4H 4L 4H 4L 4H 4L 4H
!clk 4H 4L 4H 4L 4H 4L 4H 4L 4H 4L 4H 4L
A 6H 8L 8H 2L 6H 8L 2H 6L 2H
R1
R2

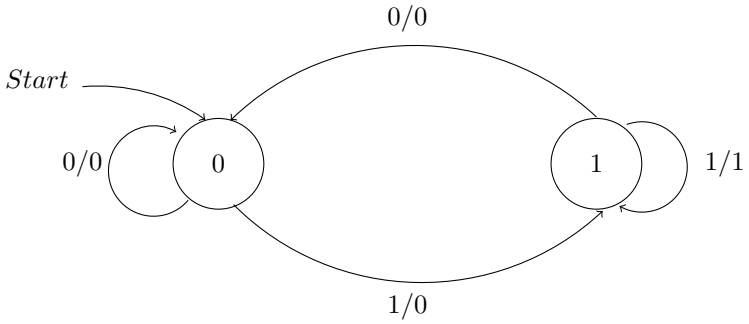
1.2 In the circuit below, RegA and RegB have setup, hold, and clk-to-q times of 4ns, all logic gates have a delay of 5ns, and RegC has a setup time of 6ns. What is the maximum allowable hold time for RegC? What is the minimum acceptable clock cycle time for this circuit, and clock frequency does it correspond to?



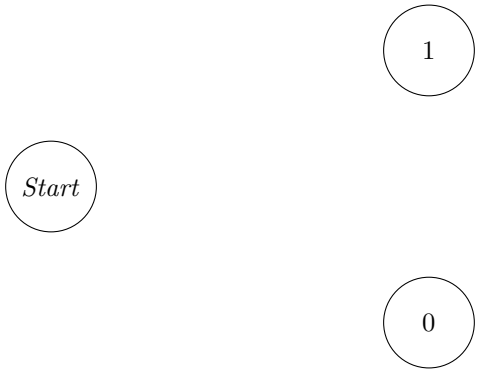
2 Finite State Machines

Automatons are machines that receive input and use various states to produce output. A finite state machine is a type of simple automaton where the next state and output depend only on the current state and input. Each state is represented by a circle, and every proper finite state machine has a starting state, signified either with the label "Start" or a single arrow leading into it. Each transition between states is labeled [input]/[output].

2.1 What pattern in a bitstring does the FSM below detect? What would it output for the input bitstring "011001001110"?



2.2 Fill in the following FSM for outputting a 1 whenever we have two repeating bits as the most recent bits, and a 0 otherwise. You may not need all states.



2.3 Write an FSM that will output a 1 if it recognizes the regex pattern {10+1}.