CS61C Spring 2025

Precheck: SDS, RISC-V Datapath

Discussion 8

1 Pre-Check: T/F?

1.1 Register "clk-to-q" delay is the time between the rising edge of the clock signal and the register's hold time.

False. "clk-to-q" delay is the time between the rising edge of the clock signal and the time it takes for the register's output to reflect the new input.

1.2 State elements only update their output on the rising edge of the clock, even if the inputs change between clock rising edges.

True. State elements will update their output on the rising edge of the clock signal. Between rising edges, the state element's output will remain constant regardless of the inputs.

1.3 The single cycle datapath uses the outputs of all hardware units for each instruction.

False. All units are active in each cycle, but their output may be ignored (gated) by control signals.

1.4 It is possible to execute the stages of the single cycle datapath in parallel to speed up execution of a single instruction.

False. Each stage depends on the value produced by the stage before it (e.g., instruction decode depends on the instruction fetched).

1.5 If the logic delay of reading from IMEM is reduced, then any (non-empty) program using the single cycle datapath will speed up.

True. Since every instruction must read from IMEM during the instruction fetch stage, making the IMEM faster will speed up every single instruction.

1.6 Stores and loads are the only instructions that require input/output from DMEM.

True. For all other instructions, we don't need to read the data that is read out from DMEM, and thus don't need to wait for the output of the MEM stage.

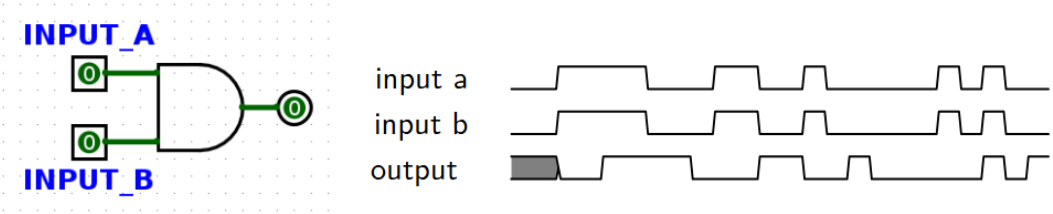
1.7 It is possible to feed both the immediate generator's output and the value in rs2 to the ALU in a single instruction.

False. You may only use *either* the immediate generator or the value in register rs2. Notice in our datapath, there is a mux with a signal (BSel) that decides whether we use the output of the immediate generator or the value in rs2.

2 SDS

There are two basic types of circuits: combinational logic circuits and state elements.

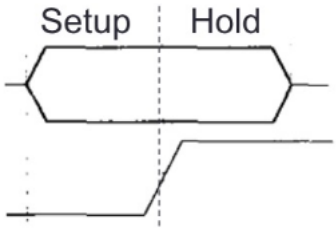
Combinational logic circuits simply change based on their inputs after whatever propagation delay is associated with them. For example, if an AND gate (pictured below) has an associated propagation delay of 2ps, its output will change based on its input as follows:



You should notice that the output of this AND gate *always* changes 2ps after its inputs change.

State elements, on the other hand, can *remember* their inputs even after the inputs change. State elements change value based on a clock signal. A rising edge-triggered register, for example, samples its input at the rising edge of the clock (when the clock signal goes from 0 to 1).

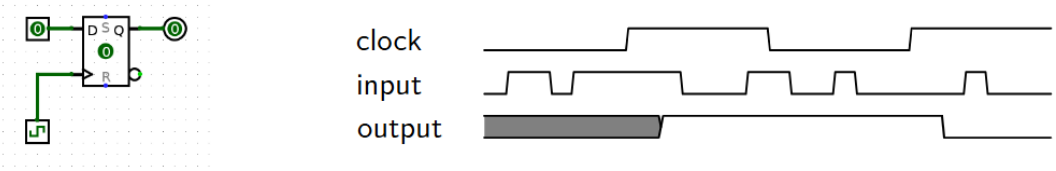
Like logic gates, registers also have a delay associated with them before their output will reflect the input that was sampled. This is called the **clk-to-q** delay. ("Q" often indicates output). This is the time between the rising edge of the clock signal and the time the register's output reflects the input change.



The input to the register samples has to be stable for a certain amount of time around the rising edge of the clock for the input to be sampled accurately. The amount of time before the rising edge the input must be stable is called the **setup** time, and the time after the rising edge the input must be stable is called the **hold** time. Hold time is generally included in clk-to-q delay, so clk-to-q time will usually be greater than or equal to hold time.

Logically, the fact that clk-to-q $\geq$ hold time makes sense since it only takes clk-to-q seconds to copy the value over, so there's no need to have the value fed into the register for any longer.

Examine the register circuit and assume **setup** time of 2.5ps, **hold** time of 1.5ps, and a **clk-to-q** time of 1.5ps. The clock signal has a period of 13ps.



Notice that the value of the output in the diagram doesn't change immediately after the rising edge of the clock. Until enough time has passed for the output to reflect the input, the value

held by the output is garbage; this is represented by the shaded gray part of the output graph. Clock cycle time must be small enough that inputs to registers don't change within the hold time and large enough to account for clk-to-q times, setup times, and combinational logic delays.

A few important SDS relationships are below:

$$\tau_{\text{critical path delay}} = \tau_{\text{clk-to-q}} + \tau_{\text{combinational logic delay}} + \tau_{\text{setup time}}$$

where $\tau_{\text{combinational logic delay}}$ is the maximum combinational logic delay for any register $\rightarrow$ register path in the circuit. The path with the maximum delay is called the "critical path".

Additionally, circuits must satisfy hold-time constraints because hold times may be violated if data propagates too quickly (see above):

$$\tau_{\text{clk-to-q}} + \tau_{\text{smallest combinational delay}} \geq \tau_{\text{hold time}}$$

3 Single-Cycle Datapath

Our single-cycle datapath is a synchronous digital system (SDS) that has the capabilities of executing RISC-V instructions. It is divided into multiple stages of execution, where each stage is responsible for a completing a certain task.

IF Instruction Fetch:

- Send address to the instruction memory (IMEM), and read IMEM at that address.
- **Hardware units**: PC register, +4 adder, PCSel mux, IMEM

ID Instruction Decode:

- Generate control signals from the instruction bits, generate the immediate, and read registers from the RegFile.
- **Hardware units**: RegFile, ImmGen

EX Execute:

- Perform ALU operations, and do branch comparison.
- **Hardware units**: ASel mux, BSel mux, branch comparator, ALU

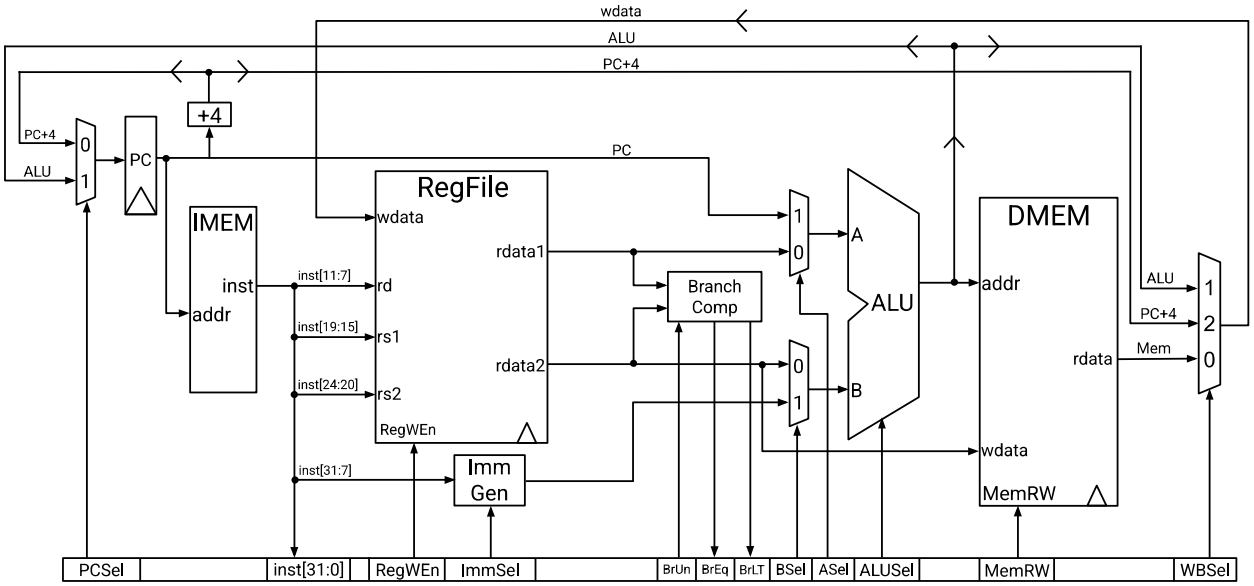
MEM Memory

- Read from or write to the data memory (DMEM).
- **Hardware units**: DMEM

WB Writeback

- Write back either PC + 4, the result of the ALU operation, or data from memory to the RegFile.
- **Hardware units**: WBSel mux, RegFile

Single-Cycle Datapath Diagram



5-Stage Datapath Diagram