CS61C Summer 2025

Precheck: RISC-V Datapath

Discussion 9

1 Pre-Check: T/F?

1.1 Register "clk-to-q" delay is the time between the rising edge of the clock signal and the register's hold time.

False. "clk-to-q" delay is the time between the rising edge of the clock signal and the time it takes for the register's output to reflect the new input.

1.2 State elements only update their output on the rising edge of the clock, even if the inputs change between clock rising edges.

True. State elements will update their output on the rising edge of the clock signal. Between rising edges, the state element's output will remain constant regardless of the inputs.

1.3 The single cycle datapath uses the outputs of all hardware units for each instruction.

False. All units are active in each cycle, but their output may be ignored (gated) by control signals.

1.4 It is possible to execute the stages of the single cycle datapath in parallel to speed up execution of a single instruction.

False. Each stage depends on the value produced by the stage before it (e.g., instruction decode depends on the instruction fetched).

1.5 If the logic delay of reading from IMEM is reduced, then any (non-empty) program using the single cycle datapath will speed up.

True. Since every instruction must read from IMEM during the instruction fetch stage, making the IMEM faster will speed up every single instruction.

1.6 Stores and loads are the only instructions that require input/output from DMEM.

True. For all other instructions, we don't need to read the data that is read out from DMEM, and thus don't need to wait for the output of the MEM stage.

1.7 It is possible to feed both the immediate generator's output and the value in rs2 to the ALU in a single instruction.

False. You may only use *either* the immediate generator or the value in register rs2. Notice in our datapath, there is a mux with a signal (BSel) that decides whether we use the output of the immediate generator or the value in rs2.

2 Single-Cycle Datapath

Our single-cycle datapath is a synchronous digital system (SDS) that has the capabilities of executing RISC-V instructions. It is divided into multiple stages of execution, where each stage is responsible for a completing a certain task.

IF Instruction Fetch:

- Send address to the instruction memory (IMEM), and read IMEM at that address.
- **Hardware units**: PC register, +4 adder, PCSel mux, IMEM

ID Instruction Decode:

- Generate control signals from the instruction bits, generate the immediate, and read registers from the RegFile.
- **Hardware units**: RegFile, ImmGen

EX Execute:

- Perform ALU operations, and do branch comparison.
- **Hardware units**: ASel mux, BSel mux, branch comparator, ALU

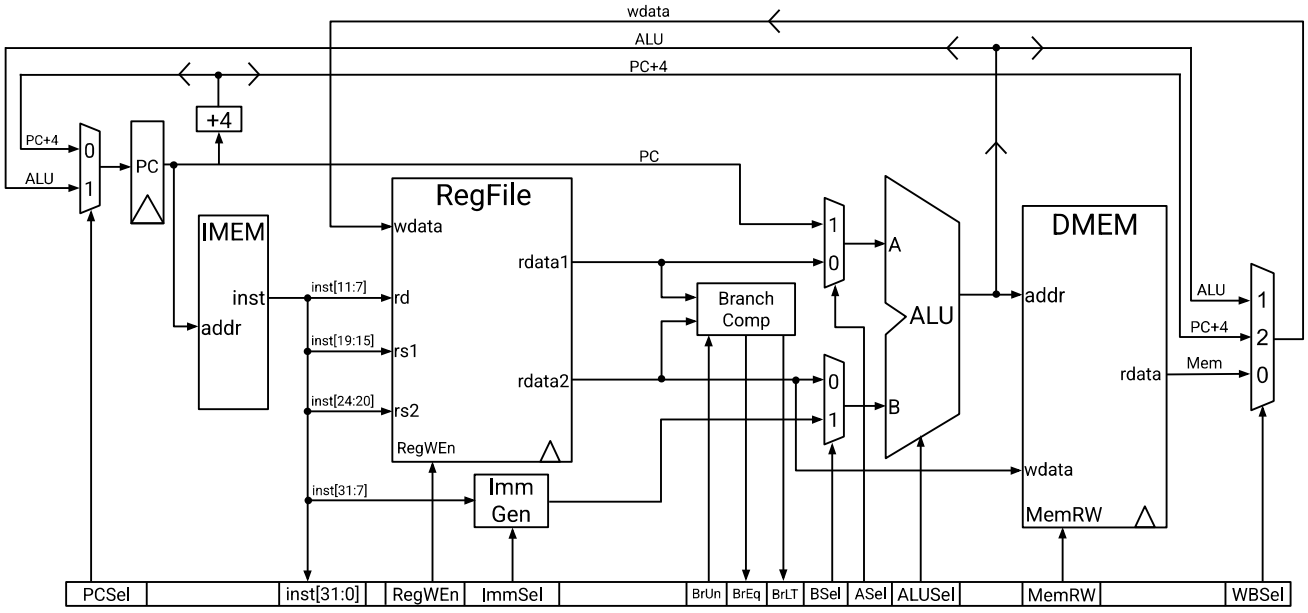
MEM Memory

- Read from or write to the data memory (DMEM).
- **Hardware units**: DMEM

WB Writeback

- Write back either PC + 4, the result of the ALU operation, or data from memory to the RegFile.
- **Hardware units**: WBSel mux, RegFile

Single-Cycle Datapath Diagram



5-Stage Datapath Diagram